Comparative Study of 4-Bit Flash ADC - Aspect Ratio, Supply Voltage and Power Consumption

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Abstract: ***With the advancement in technology, the sensor demand has increased and this works with the device which converts the continuous data into discreate data. In the proposed work, we are comparing the performance parameters of various technologies for a 4 Bit Analog to Digital Converter. The comparison was done mainly on nano-meter technologies used in designing the circuit. The performance metrics like power consumption and sampling frequency are compared. Initially the flash ADC is being compared to other types of ADC's. Then we compared different system architectures of 4 Bit Flash ADC and measured its performance.***

Key words: Analog to Digital Converter, Nano-Meter, flash ADC, Successive

1. INTRODUCTION

In the recent high-tech world, the signals are analogous in nature such as sound, radio, light waves etc. Whereas, in the digital world there are only ones and zeros, which are called as bits. These several bits put together form a number. As told earlier the signals in physical world are continuous and analogous, for further processing these signals are sampled to bits. This type of conversion is termed as Analog to Digital Conversion, and an Analog to Digital Converter [ADC] is used for the same data conversion purpose. Thus, the conversion of Continuous to Discrete Data is an important block in a signal processing systems and mixed signal design application.

There are variety of ADCs used, depending on the type of signal to be sampled which are flash ADC, sigma-delta ADC, dual slope converters, successive approximation ADC(SAR), counter type ADC etc, which have their own distinctive characteristics and limitations. Sigma-delta ADC samples an analog signal with a sampling frequency and subsequently quantizes into a digital signal in a multi-level quantizer. The output of Dual slope ADC is equal to analog data, which is calculated using two slopes of the data. The performance of a Counter ADC depends on the counter operation used in the circuit. A SAR ADC works with the principle of binary search through all possible quantization levels.

The distinctive type of ADC which is fastest compared to the others is Flash ADC, because the signal conversion is performed through a set of comparators simultaneously. Flash ADC works on the principle of comparing analog input voltage with a set of reference voltages. Typical time conversion in this type is 100ns or less. The construction of Flash ADC is easy and simple. They are used in high frequency sensor-based applications because the high sampling rate. A 4 Bit Flash ADC is more preferred over the other bits because the number of comparators used is less, the circuit is smaller in size and simple, reducing the cost of production. And these circuits can be further used for developing higher ADC bits. Designing a higher bit ADC requires more number of comparators, as the number of bits increase the count of the comparator gets doubled every time leading to a complex circuit.

The proposed study aims at designing an IC for 4-bit Flash ADC in the field of VLSI. For designing an IC an important factor is the technology to be used which varies from micrometer to nano-meter, and nano-meter technology is presently used in the industry level designing of circuits. Nano-meter technology used for designing the Flash ADC mainly talks about the aspect ratio which is the width of the CMOS channel which determine the power dissipation of the circuit. The technologies widely used are 45nm, 90nm and 180nm. The Flash ADC has comparators and encoders as the primary building blocks. In the Conventional Flash ADC, the comparators require the reference voltages for

comparing which is provided by the resistor bank. Comparator estimates the similarities between the reference voltage that is supplied by the resistor network and the input voltage signal. The output of a comparator is '1' when the voltage applied is more than the reference and is '0' when applied voltage is less than the reference. The required comparators used in designing a flash ADC is generally [2^n]-1. The output generated by the comparator is of the form thermometer code. Thermometer code is series of 0's followed by 1's, where 1's in the output code increases as the input voltages increases. Added advantage is that glitches are removed. However, for obtaining the output in the form of binary code, this thermometer coded has to be encoded.

2. LITERATURE SURVEY

A 4-bit Flash ADC [1] is designed by Ramyashree and Satheesh, the system is built using Inverter Threshold Comparator and Binary Encoder. A 45nm technology was used to design the system. Threshold Modified Comparator Circuits modified to get [2] Inverter Threshold Comparator (ITC), it is implemented by changing the aspect ratio of the inverter and works with voltage of 1.1 V and frequency of 100 kHz, consumes a power of 16.82µW. This design is proposed by Vivek et al. Abdulla et al. proposed a 4-bit flash ADC built on the architecture of a StrongARM comparator [3] which is an alternative for the existing ladder. The size of the comparator's input differential amplifier pair is altered systematically for improving the design. A new circuit called the Helpee Strong ARM circuit, is used to allow the operation of the device at the voltages which are below the transistor's threshold voltage. Thermometer code from the Strong ARM is converted using a 1-out-of-15 decoder, while the 1-out-of-n code is converted using a Helpee Strong ARM. Standard 90nm CMOS technology is used to simulate the system, which operates at the frequency of 1.6 GHz, and consumes 292 µW.

A multiplexer-based code converter for 4 Bit Flash ADC that transforms thermometer to binary code was proposed by Mayur S. For conversion, the system employs a 2:1 mux [4] and two input XOR gates. To convert the thermometer code to comparable grey code, 2:1 Mux is initially used. XOR gates are used to convert the resulting code to binary code. In comparison to the existing conventional system, the proposed design reduces power consumption with grounding concept and eliminates the need for additional inverters. The encoder is designed using 180 nm CMOS technology, with N-well technology operating at 1.8V. The comparator gain is increased by using a buffer at the system's end, and the system's speed is reduced by using an additional delay clock. Malathi et al. developed a modified design for a inverter-based comparator [5] that utilizes only one clock signal to reduce the latency. This system can also be utilised as a thermometer to binary code converter because the given analog input is first transformed to grey code and then to binary code. The system operates at 100 MS/s of sampling rate which is a maximum value and has an input signal with a 1.8 V swing, and consumes 1.08 mW of power. Xuan et al. developed a 4 bit Flash ADC having a single-core and operating at 40 GS/s using a 130nm SiGe Bi-CMOS technology. The converter utilises a travelling wave approach [6] moreover, the design includes new Pseudo-XOR grey encoder having the low complexity. The system operates at 39.04 GS/s and incorporates folded-cascode differential logic.

Yulang et al. developed a 4-bit flash Analog to Digital Converter using a 28 nm Fully Depleted Silicon on Insulator CMOS technology having a sampling rate of 25GS/s. The Track-and-Hold bandwidth process is thoroughly investigated, with a single-core ADC design guideline aiming for cutting-edge speed performance [7].The power consumption is reduced by using De-mux comparator which is based on 1-to-2 Strong Arm latch along with a fat-tree encoder which is used for thermometer to binary code conversion and a body biasing. In conventional 65nm CMOS technology, Bayan Nasri et al. developed a low-power 4-bit folding-flash ADC having 2 has a folding factor and sampled at 1GS/s. A new dynamic comparator which is unbalanced and double tailed with a high dynamic range and ultra-low power [8] operation has been developed. The

design has a input stage that is fully matched, an latch stage which is unbalanced, and two clock operation strategy, as opposed to traditional approaches. The integration of all these components results in the reduction of the kick-back noise while also enabling flexibility of the design to change the comparators' trip-points. Kriti and Sandeep proposed a 4bit Hybrid Flash ADC that employs a sequence of resistances, a 2^[n-1] comparators, and an encoder based on mux [9]. The 4bit Flash Converter was developed and simulated using a 90nm technology with a 1.2 V of supply voltage and 1GHz of frequency. The designed Flash ADC is more stable and consumes less power. Mirosalva et al. described a 4-bit Flash ADC design for Ultra-Wideband sensor systems [10]. In 350 nm SiGe Bi-CMOS technology, the converter cell structure was designed and fabricated. With a maximum input signal range of 1.6 Vpp at 1 MHz, the converter cell can achieve up to 1.1 Gs/s. The developed cell's power consumption from a -3.3 V power supply is 30 mA.

Zbigniew proposed the design of a 4-bit Flash type analog to digital converter in 22 nm technology with 0.8 V of supply voltage. This block is a part of the original sub-ranging converter, which works on the assumption [11] that sub-ADC and sub-DAC have good linearity while their nominal resolutions remain low. The comparator design has a resolution of ±1.5MV, which was achieved by utilising the Fully Depleted Silicon on Insulator (FD-SOI) process' ability to trim the threshold voltage of the transistor by modifying the back gate polarisation. The system operates at a 500 Ms/s sampling rate. Ms/s. Hazrat and Raghavendra discussed a Flash ADC that uses a comparator which is dynamic and consumes a power of 0.169uW. And an encoder block that is designed using a 2 is to 1 mux. With these components, a 4-bit Flash converter dissipates 7.2394mW of power and provides a latency of 29.792ns. The same design was tested for functionality [12] and 180nm Technology was used to implement the design. Shylu et al. developed the circuit of a 4-bit Flash converter aiming at consuming less power for high-frequency applications. The Flash ADC's power consumption has been decreased in two phases: in step one, a low-power dynamic comparator [13] has been built, and in phase two, a low-power Fat tree encoder has been designed. In comparison to traditional encoder designs, the encoder design employs fewer gates. As a result, the encoder block's average power dissipation is 43.6 μW, and it was constructed using 90nm technology. At a 1V power supply and a sampling frequency of 1GHz, the entire system consumes 5.1096 mW of power.

Mayur et al. presents a low-power standard cell based 4-bit flash ADC with a sampling rate of 400MS/s [14]. The converter employs logic gate-based comparators. The output of the comparator is defined to be ‘1’ or ‘0’ by the comparision between the input voltage and the comparator’s reference voltage. The gain booster and encoder come after the comparator. By successfully transitioning the comparators to standby mode from active, low power consumption is accomplished. The signal termed as a control signal determines the switching activity. This ADC is built in 180 nm N-well technology at the transistor level with input voltage of 1.8 V and 3.9 mW of power consumption. Triveni and Das have made a concerted effort to reduce noise while also increasing the speed of circuit. The circuit is of a mixed signal design. This research aimed to improve the architecture of a Quantum-Voltage Comparator (QVC) used in a 4-bit flash ADC, resulting in reduction of the noise and linearity [15]. The ADC's decoder based on 2x1 multiplexer boots the speed of the design. QVC reduces the ladder of resistors which were used in a traditional ADC by cascading two differential-comparators as one comparator by changing the NMOS pair sizes.

3. PROPOSED STUDY

	Technology [nm]	System Architecture	Supply Voltage	Power (mW)	Sampling frequency
[1]	45nm	Resistor ladder, Comparators, buffers and a Thermometer Encoder circuit.	2.5 V	9mW	900KHz
[2]	45nm	Invertor Threshold Comparator and the Binary Encoder (2:1 mux using pass transistor logic)	1.1 V	0.016mW	100 KHz

Table 1: Comparison of circuit performance in 45nm technology

A comparative study of parameters in 45nm technology is shown in table 1. It is observed that power consumption is depending upon the supply voltage wherein supply voltage is purely dependent on the system architecture. In [1] a comparator is designed using a 2 Stage Operational Amplifier for lower power consumption and a thermometer to binary encoder for generating binary output similar to outputs produced in a thermometer. [2] uses Inverter Threshold comparator for minimizing the power as well as area along with binary encoder for translation of thermometer code to equivalent binary code. Here, invertor threshold comparator is a modified version of conventional comparator aiming to reduce the power consumption. It is observed that high power is consumed in [1] than [2] because of the usage of resistor ladder which provides reference voltage for the comparator. High power consumption in [1] because of high supply voltage causes the conversion rate to be higher when compared to [2]. So, it can be concluded system architecture and supply voltage play a major role in low power consumption of the circuit.

Table 2: Design parameters compared in 90nm technology

	Technology [nm]	System Architecture	Supply Voltage	Power [mW]	Sampling Frequency
[1]	90nm	StrongARM and HelpeeStrongARM comparators and an Enhanced 1-out-of-15 Decoder.	Rail to Rail	0.292mW	1.6 GHz
[2]	90nm	Resistor ladder, Double Tail Comparator, Encoder.	1.2 V	1.4mW	1 GHz
[3]	90nm	Resistor Ladder, Dynamic Comparator, Fat Tree Encoder.	1 V	5.1096mW	1 GHz

Relation between the design parameters with respect to 90nm technology is shown in table 2. Rail to Rail input mentioned in [3] is a voltage range which includes both positive and negative voltage range. Strong ARM and Helpee Strong ARM comparators are used for covering the voltage range Vin > Vth and for the voltage range Vin < Vth, respectively. Because the input is rail-to-rail. When compared to conventional design these consume less energy and offers better performance. Hence, [3] consumes less power and has high conversion rate. Power consumption in [9] is comparatively lesser than [13] having a similar supply voltage is because of different system architecture in [13] which includes Fat Tree code Encoder. Fat Tree Encoder works in two stages for encoding thermometer code to binary code whereas the former converts the code in single stage. From table 2, it can be concluded from the overall comparision that using rail to rail supply for the comparator designed using Strong ARM

and the Helpee Strong ARM [1] consumes less power in 90nm technology without the resistor ladder.

	Technology [nm]	System Architecture	Supply Voltage	Power (mW)	Sampling Frequency
[14]	180nm	Resistive ladders, Standard cell comparator, Encoder	1.8 V	3.9mW	0.4 GHz
	180nm	Quantum Voltage Comparator [QVC], SNR	1.8 V	4.19mW	5.2 GHz
[4]	180nm	Comparator and Thermometer to Binary code Encoder.	1.8 V	0.025mW	1.9 GHz
[5]	180nm	Modified Inverter Comparator, Gray to Binary converter	1.8 V	1.08mW	0.1GHz
[12]	180nm	Resistor Ladder, Dynamic Comparator, Encoder	NM	7.2394mW	33.56 GHz

Table 3: Study of performance parameters of 180nm technology

Here it can be observed that in spite of having same supply voltage [14], [15], [4], [5] the conversion rate and power dissipated are different. [4] consumes less power compared to other designs is because of the new design of the encoder using MUX. It reduces the power consumption by 60% when compared to Wallace Tree encoder. Wallace tree encoder counts the number of 1s in the input thermometer code and has a disadvantage of large delay and power. [5] directly converters analog input to gray code using window comparator and later converts to binary output using high speed six transistor exor gates. Hence, consumes more power compared to [4]. In [15] Quantum Voltage Comparator was used for the improvement in accuracy and noise immunity of the overall ADC circuit and did not lay focus on power consumption. Thus, it can be concluded that system architecture plays a vital role in determining the power consumption. Aiming to increase the conversion rate [12] dissipates more power. Hence a compromise should be made between power dissipation and sampling frequency.

Table 4: Performance parameters of various technologies

	Technology [nm]	System Architecture	Supply Voltage	Power (mW)	Sampling Frequency
[11]	22 nm	FD-SOI technology with 0.8V supply voltage.	0.8V	NM	0.5GHz
[7]	28nm	Resistor ladder, sample and hold circuit, comparator [preamplifier + strong arm latches], fat tree encoder.	NM	440mW	25 GHz
[8]	65nm	Track and hold circuit, 1bit folding stage, 3 Bit ADC, DFF and encoder.	1 V	0.7mW	1 GHz
[6]	130nm	ADC core [contains input driver, clock driver, reference ladder, comparator], Gray Encoder, Scrambler, PRB, FD, mux	NM	0.022mW	40.32 GHz
[10]	350nm	RC resistor network, comparator, MSD flipflop, output buffer array [double CMOS inverter].	1.6 V	30mW	0.11GHz

Power dissipation and sampling frequencies of other different technologies is compared in table 4. In [7] the circuit needs to work at 25 GS/s hence, StrongARM latches and 1-to-2 demux based comparators are used which leads to high power consumption when compared to others. [6] uses Pseudo-Exclusive-OR (PXOR) gate in place of XOR gate for enhancing the speed and reducing the power in it's encoder circuit, which uses folded-cascode differential logic. Thus, the power consumption is less when compared to other designs. In [8] when supply voltage is 1V power dissipated is less compared to [10] where supply voltage is 1.6V having a difference in the technology. Hence, it can be concluded that for [8] and [10] power dissipation depends on the supply voltage along with aspect ratio.

CONCLUSION

Relation of supply voltage and power dissipation with respect to different technologies is shown in table 5. The conclusion drawn from the comparative study of main technologies 45nm, 65nm, 90nm and 180nm depicts that power dissipation decreases with the decrease in the width of the CMOS channel, having the supply voltage ranging from 1-1.8V, the same is shown in figure 1 and figure 2. The 45nm differs from other VLSI technologies with the increase in the switching speed of the transistor when compared to others along with the reduction in the size of transistor and cost of production. Thus, 45nm technology is suitable for the circuit aiming at low power consumption compared to other technologies. The next development will be designing a 4 Bit Flash ADC in 45nm technology with a suitable design aiming for lower power consumption.

Table 5: Conclusion table for performance parameters w.r.t to various technologies.

Technology	Supply Voltage (V)	Power Consumption (mW)
45nm	1.1	0.016
65nm	1	0.7
90nm	1.2	1.4
180nm	1.8	3.9

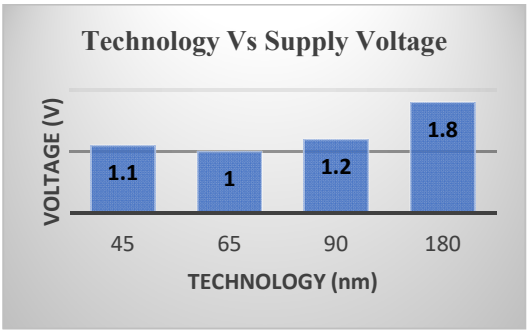

Figure 1: Technology used vs supply voltage

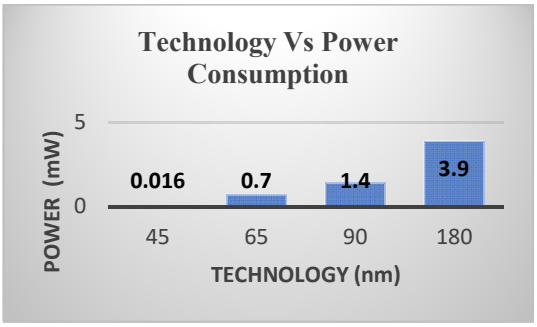

Figure 2: Technology used v/s power consumed

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